This listing of claims replaces all prior versions and listings of claims in the application.

In the Claims:

1. (currently amended) A field effect transistor ("FET"), comprising:

a single-crystal semiconductor region of a substrate, said single-crystal semiconductor region having a first composition;

a gate ~~stack~~ overlying ~~a~~ said single-crystal semiconductor region; ~~of a substrate, said single-crystal semiconductor region having a first composition~~

a pair of first spacers ~~disposed over~~ overlying respective opposite sidewalls of said gate ~~stack~~;

a pair of regions consisting essentially of a single-crystal semiconductor alloy having a second composition different from said first composition, said semiconductor alloy regions disposed on opposite sides of said gate ~~stack~~, each said semiconductor alloy region spaced a first distance from said gate ~~stack~~; and

~~a pair of~~ a source region and a drain region at least partly disposed in respective ones of said semiconductor alloy regions, each of said source region and said drain region being ~~each~~ spaced a second distance from said gate ~~stack by a first spacer of said pair of first spacers~~, said second distance being different from ~~the~~ and independent from said first distance, said second distance being at least partly determined by spacings of said first spacers from said sidewalls of said gate.

2. (currently amended) The FET as claimed in claim 1, wherein said second distance is ~~longer~~ greater than said first distance.

3. (original) The FET as claimed in claim 2, wherein said single-crystal semiconductor region consists essentially of silicon and said semiconductor alloy regions consist essentially of silicon germanium.

4. (original) The FET as claimed in claim 3, wherein said silicon germanium regions are at least partly disposed in trenches disposed in said single-crystal silicon region.

5. (original) The FET as claimed in claim 4, wherein said substrate is a silicon-on-insulator (SOI) substrate and said single-crystal silicon region is disposed above a buried oxide layer of said SOI substrate.

6. (original) The FET as claimed in claim 5, wherein said silicon germanium regions have bottom edges disposed at a depth of about 80% or greater of a depth of a top of said buried oxide layer from a top surface of said single-crystal silicon region.

7. (original) The FET as claimed in claim 6, wherein the depth of said bottom edges is about 90% of the depth of said top of said buried oxide layer.

8. (original) The FET as claimed in claim 7, further comprising extension regions underlying said first spacers and at least partly underlying said gate stack.

9. (currently amended) The FET as claimed in claim 8, further comprising halo regions underlying ~~sad~~ said first spacers and at least partly underlying said gate stack.

10. (original) The FET as claimed in claim 8, wherein said sidewalls of said gate stack are oxidized, wherein said first spacers are disposed over said oxidized sidewalls.

11. (original) The FET as claimed in claim 10, further comprising forming second spacers disposed laterally outward from said first spacers.

12. (currently amended) The FET as claimed in claim 11, further comprising silicide regions overlying said silicon germanium regions, wherein said silicide regions are spaced a distance from said gate at least partly determined by spacings of ~~spaced from said gate stack by said first spacers and~~ said second spacers from said gate.

13. (original) The FET as claimed in claim 12, wherein said gate ~~stack~~ includes a gate silicide region and a polycrystalline semiconductor region, said gate silicide region overlying and self-aligned to said polycrystalline semiconductor region.

14. (currently amended) A field effect transistor ("FET"), comprising:

~~a gate stack overlying~~ a single-crystal silicon region of a silicon-on-insulator substrate;

a gate overlying said single-crystal silicon region;

a pair of first spacers disposed over opposite sidewalls of said gate ~~stack~~;

a pair of regions consisting essentially of single-crystal silicon germanium disposed on opposite sides of said gate ~~stack~~, each said silicon germanium region spaced a first distance from said gate ~~stack~~;

~~a pair of~~ a source region and a drain region at least partly disposed in respective ones of said silicon germanium regions, each of said source region and said drain region ~~each~~ being spaced a second distance from said gate ~~stack by a first spacer of said pair of spacers~~, said second distance being different from and independent from said first distance, said second distance being at least partly determined by spacings of said first spacers from said sidewalls of said gate; and

silicide regions, at least one of said silicide regions overlying a semiconductor portion ~~disposed as a layer~~ of said gate ~~stack~~, and ~~at least ones of~~ said silicide regions at least partly overlying said silicon germanium regions.

15-30. (canceled)

31. (new) The FET as claimed in claim 1, wherein said second distance is less than said first distance.

32. (new) The FET as claimed in claim 1, wherein said single-crystal semiconductor alloy includes at least two semiconductor materials and a percentage amount of at least one of said semiconductor materials varies between said first and second compositions.